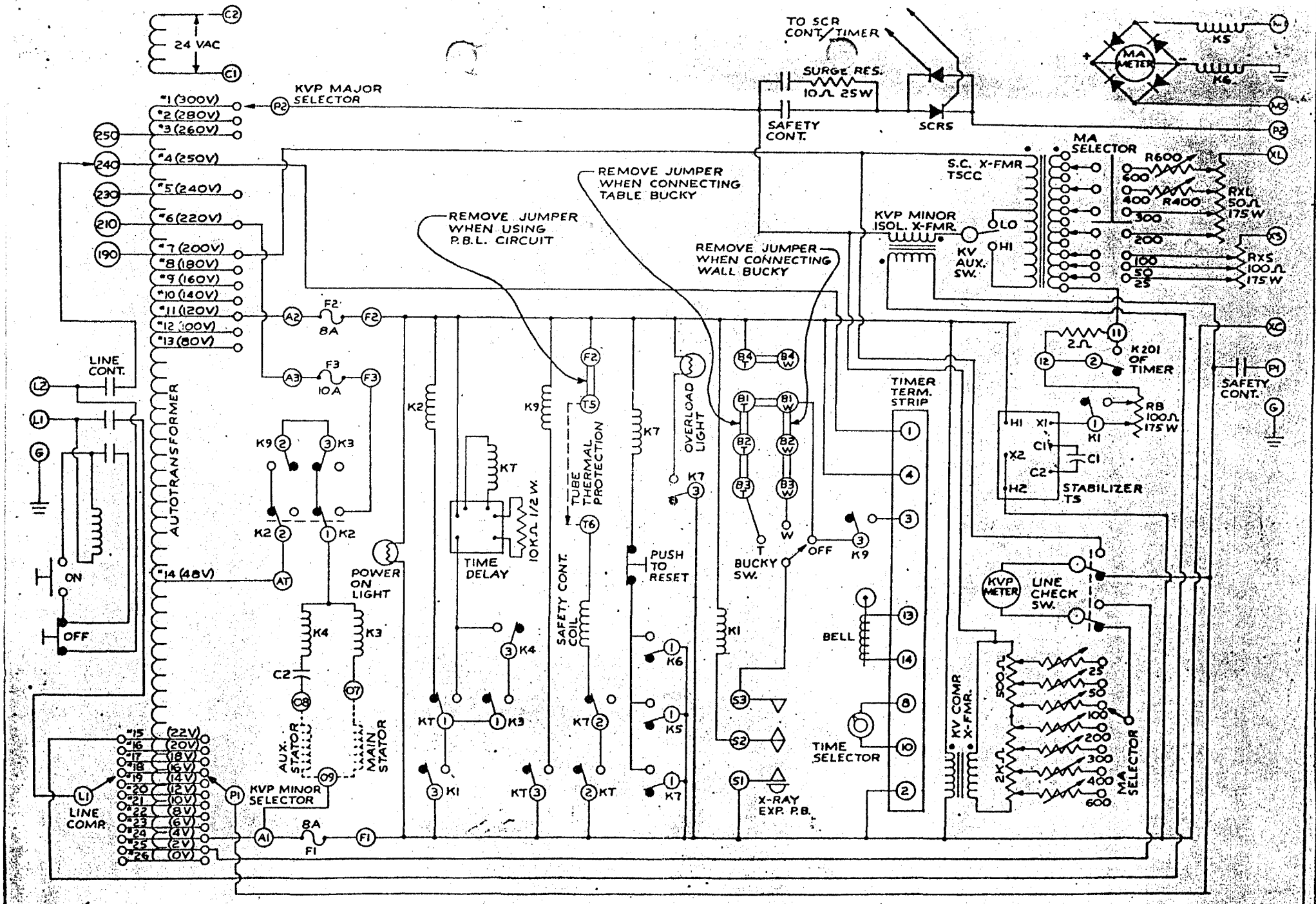
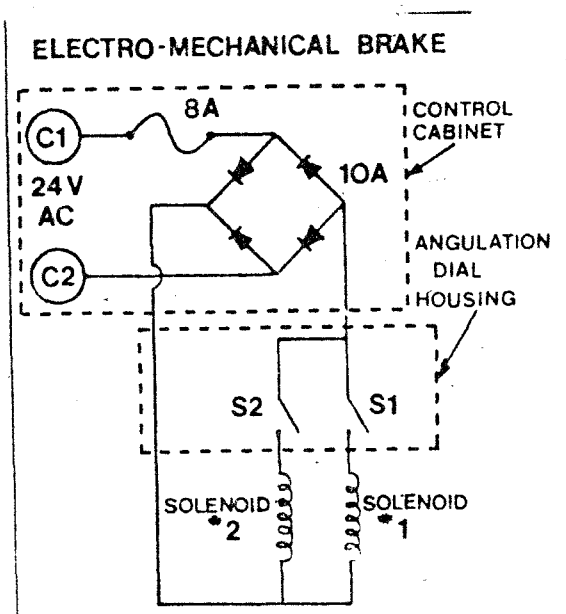


UNIVERSAL X-RAY INC. 4014 W. GRAND AVE. CHICAGO, ILL. 60651 U.S.A.

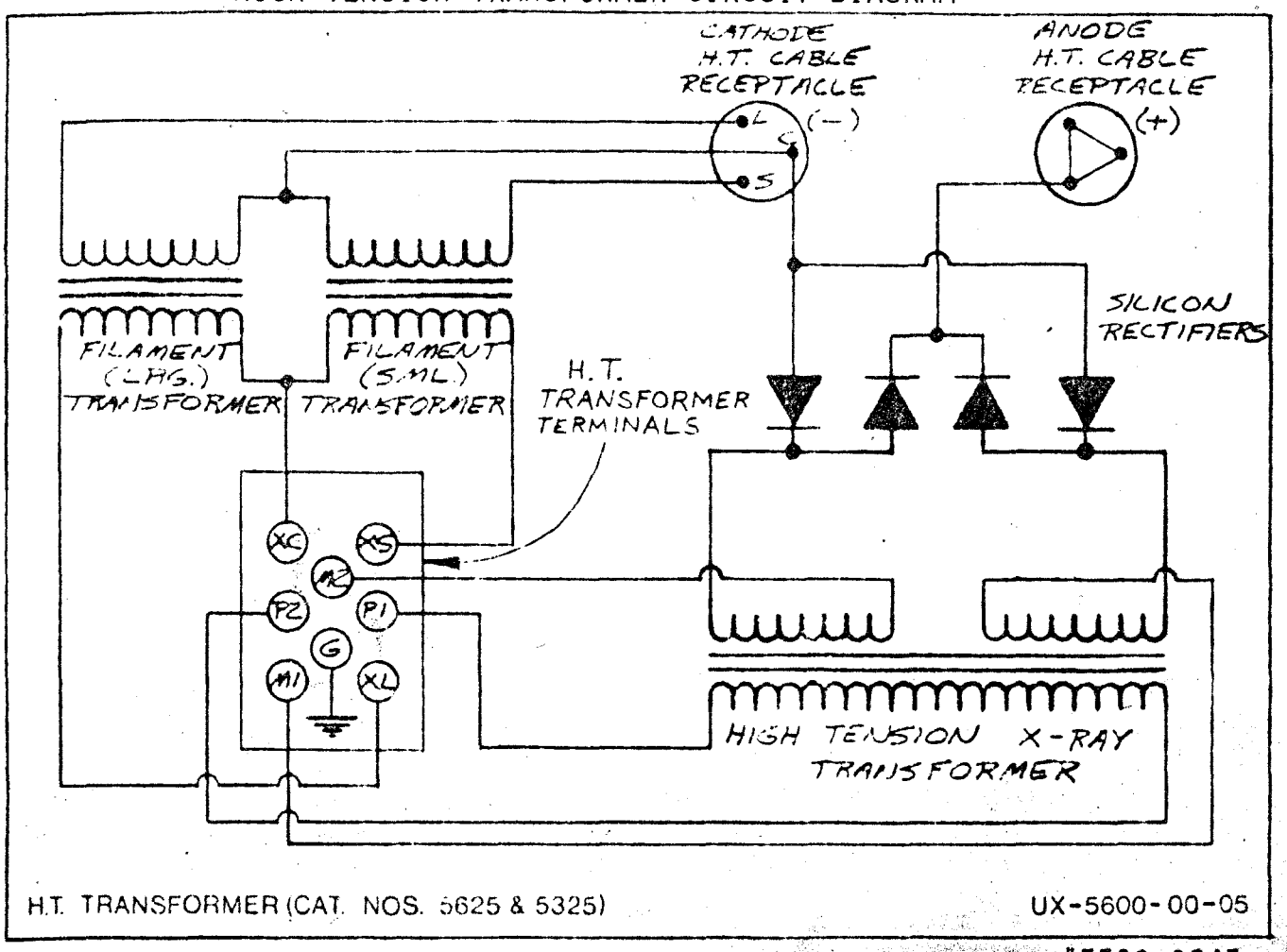
UX5600-00-06

UNIMASTER 625 CONTROL (CAT. NO. 5600) 062981

#5500-0345



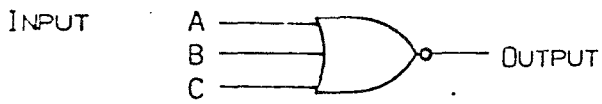
HIGH TENSION TRANSFORMER CIRCUIT DIAGRAM



H.T. TRANSFORMER (CAT. NOS. 5625 & 5325) UX-5600-00-05

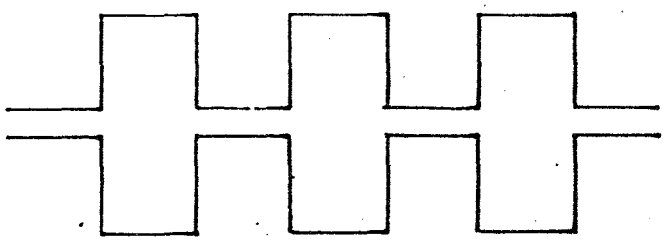
SOLID STATE LINEAR X-RAY CONTACTOR/TIMER MODULE:
THE LOGIC AND CONTROL CIRCUITRY FOR THIS MODULE WAS DESIGNED WITH NPN POSITIVE DISCREET LOGIC. THE TRUTH TABLE FOR A NOR GATE IS AS SUCH:

INPUTS			OUTPUT
A	B	C	
0	0	0	1 (HIGH)
1	0	0	0 (LOW)
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

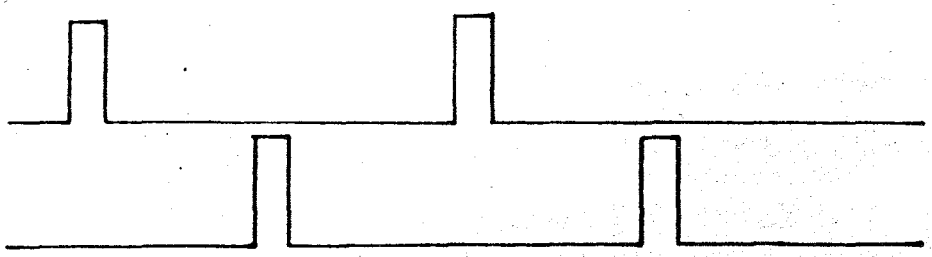


THE SEQUENCING OF EVENTS OCCURES WITH AN EXPOSURE CONTACT CLOSURE AT PIN 24 OF THE SCR TIMER P.C.B. THIS OCCURS WHEN RELAY $K_{20;}$ IS ACTIVATED. A NO (NORMALLY OPEN) CONTACT FROM THIS RELAY IS USED TO START THIS SEQUENCING AND ALSO THE TWO BACK-UP CONTACTORS ARE PULLED IN AT THIS TIME.

TWO COMPLEMENTARY SIGNALS ARE GENERATED THAT ARE SYNCHRONOUS TO THE LINE VOLTAGE PHASE, THESE SIGNALS AT THE COLLECTORS OF Q3 AND Q4 ARE:

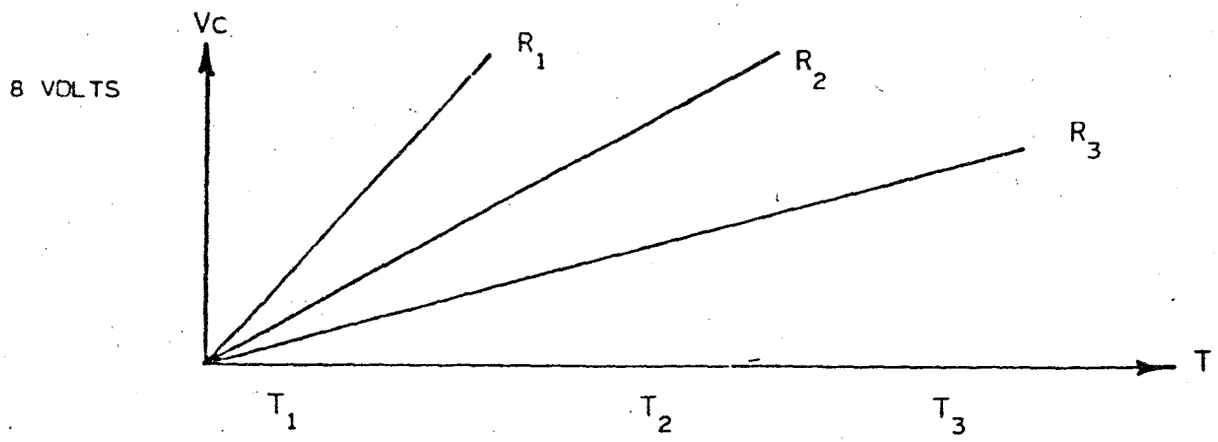


THESE SIGNALS ARE DIFFERENTIATED (C_1 AND C_2) AND AMPLIFIED AND ARE DESIGNATED L (LINE) AND $\bar{L}$ (LINE NOT), AND OCCUR EACH 16.7 MILLISECONDS.



ALL DIGITAL SIGNAL PROCESSING IS DONE WITH L AND $\overline{L}$. NOR GATES 9 AND 10 ACT AS A FLIP-FLOP AND ARE CONDITIONED BY L AND $\overline{L}$ WHEN THE INHIBIT BUS (CR_1 AND CR_2) IS LIFTED. THE TWO OUTPUTS OF THIS FLIP-FLOP ARE THE DRIVING SIGNALS FOR TRANSISTORS Q_{14} AND Q_{15}, WHICH DRIVE THE PRIMARY WINDING OF THE PULSE TRANSFORMER TR-2. THE TWO SECONDARY WINDINGS OF TR-2 DRIVE THE GATES OF SCR'S THAT ARE IN SERIES WHTIH THE HIGH-TENSION TRANSFORMER. WHEN THESE SCR'S ARE TURNED ON, THE X-RAY OUTPUT IS ACHIEVED THROUGH THIS HIGH-TENSION TRANSFORMER.

WHEN THE MERCURY WETTED RELAY K_E IS ACTIVATED, A CONTACT CLOSURE K_E APPLIES AN INTEGRATED SIGNAL TO TRANSISTOR Q_1 TURNS ON, AND WHEN Q16 IS CONDITIONED, THEN NOR GATE 17 IS TURNED OFF. THIS GIVES A START OF COUNT TO THE LINEAR TIMER, SINCE THE TWO INHIBITS CLAMPING THE TIMER ARE NOW LIFTED (CR_2 AND CR_8). THE CAPACITOR C_2 NOW CHARGES UP IN A LINEAR SLOPE DUE TO THE CONSTANT CURRENT SOURCE ESTABLISHED BY Q_3 AND THE PROGRAMMED EXTERNAL TIMING RESISTOR.



THIS TIMING CAPACITOR WILL CHARGE UP TOWARD THE +15 VOLT SUPPLY ESTABLISHED BY THE ZENER ACTION OF CR_3. THE FET SOURCE FOLLOWER ACTS AS AN UNLOADED OUTPUT AND TRANSISTORS Q_5 AND Q_6 ACT AS A TRIGGER THAT IN TURN GATES NOT 12 TO FORM AN END OF COUNT. THE TRIGGER IS SET AT APPROXIMATLEY 8 VOLTS OF CHARGE ON THE TIMING CAPACITOR.

AT THE END OF COUNT, THE GATE PULSES TO THE SCR'S IS DISCONTINUED AND THE EXPOSURE TIME IS ENDED.

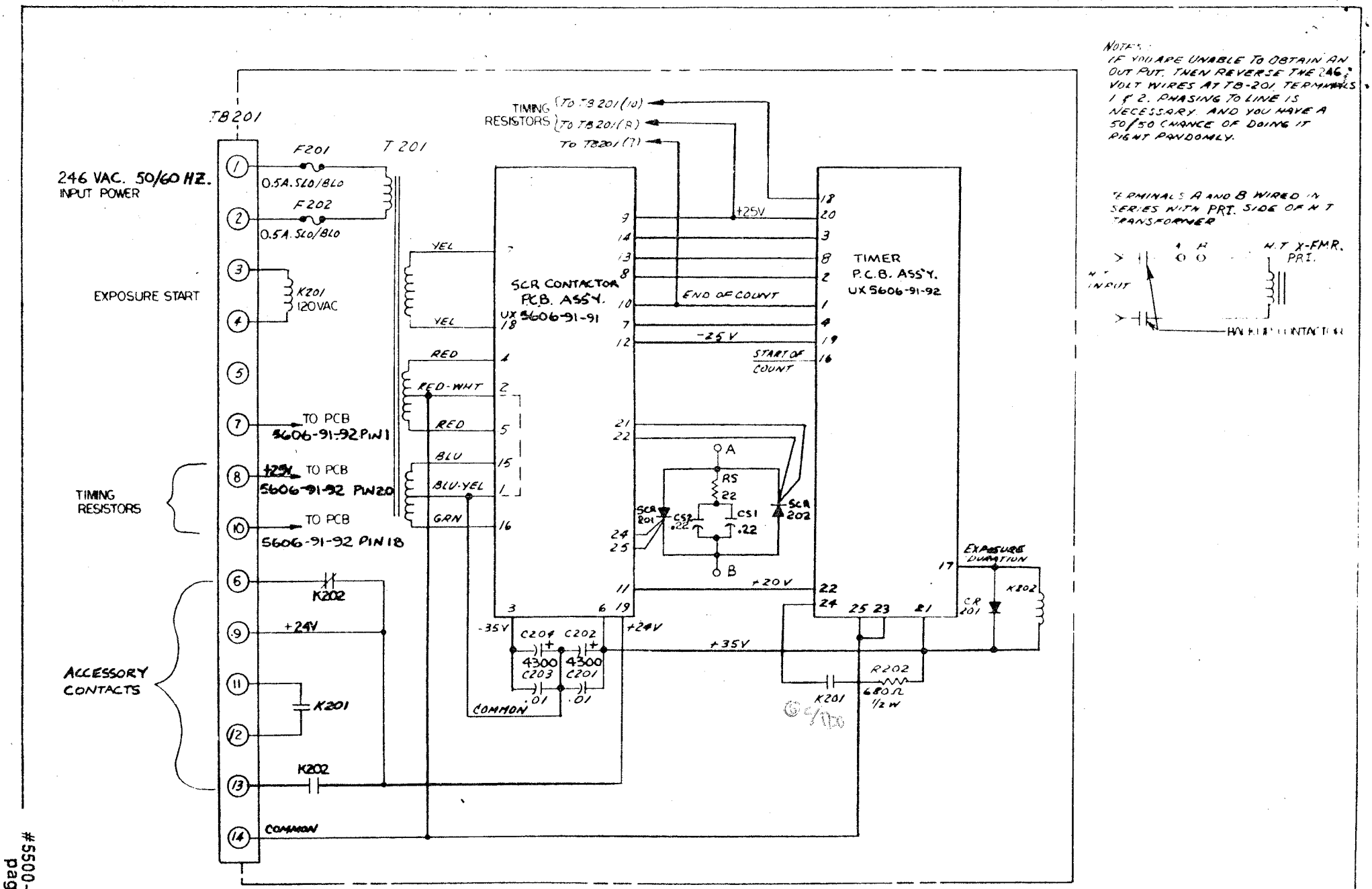
NOR GATES 17 AND 18 ACT AS A FLIP-FLOP, AND THE START OF COUNT SIGNAL (NOR 17 GOES HIGH) IS ACHIEVED WHEN Q_1 TURNS ON AND Q_{16} IS CONTINUED. THIS HAPPENS WHEN A DIFFERENTIATED PULSE FROM EITHER C_3 OR C_4 IS " OR" GATED THROUGH CR_6 OR CR_7 AND TURNS ON Q_{15}. THE DIFFERENTIATED PULSE IS ACHIEVED WHEN THE FLIP-FLOP FORMED BY NOR 9 AND NOR 10 IS TOGGLED. THIS FORMS THE BASIS FOR THE "CORE MEMORY" OF THE UNIT.

NOR GATES 7 AND 8 ARE SLAVED TO THE LINE AND LINE NOT SIGNALS. THEY ALSO FORM A FLIP-FLOP. THEIR OUTPUTS ARE USED TO CONDITION NOR GATES 9 AND 10 TOGETHER WITH THE OUTPUTS OF NOR 9 AND 10 OF THE CONTACTOR P.C.B., AND THE OUTPUT OF Q_1.

THE CORE MEMORY IS ACHIEVED DUE TO THE RELATIONSHIP OF THE OUTPUTS OF NOR 9 AND NOR 10 TO THE DRIVING TRANSISTORS Q_{14} AND Q_{15} WHICH EITHER SET OR RESET THE CORE OF THE TR2 PULSE TRANSFORMER. A SET (Q_{14} ON) WILL FIRE ONE OF THE TWO SCR'S, AND A RESET (Q_{15} ON) WILL FIRE THE ALTERNATE SCR. THE ASSOCIATED SCR CONDUCTION IN RELATION TO THE LINE VOLTAGE IS THE BASIS FOR THE " CORE MEMORY" .

TIMING RESISTORS

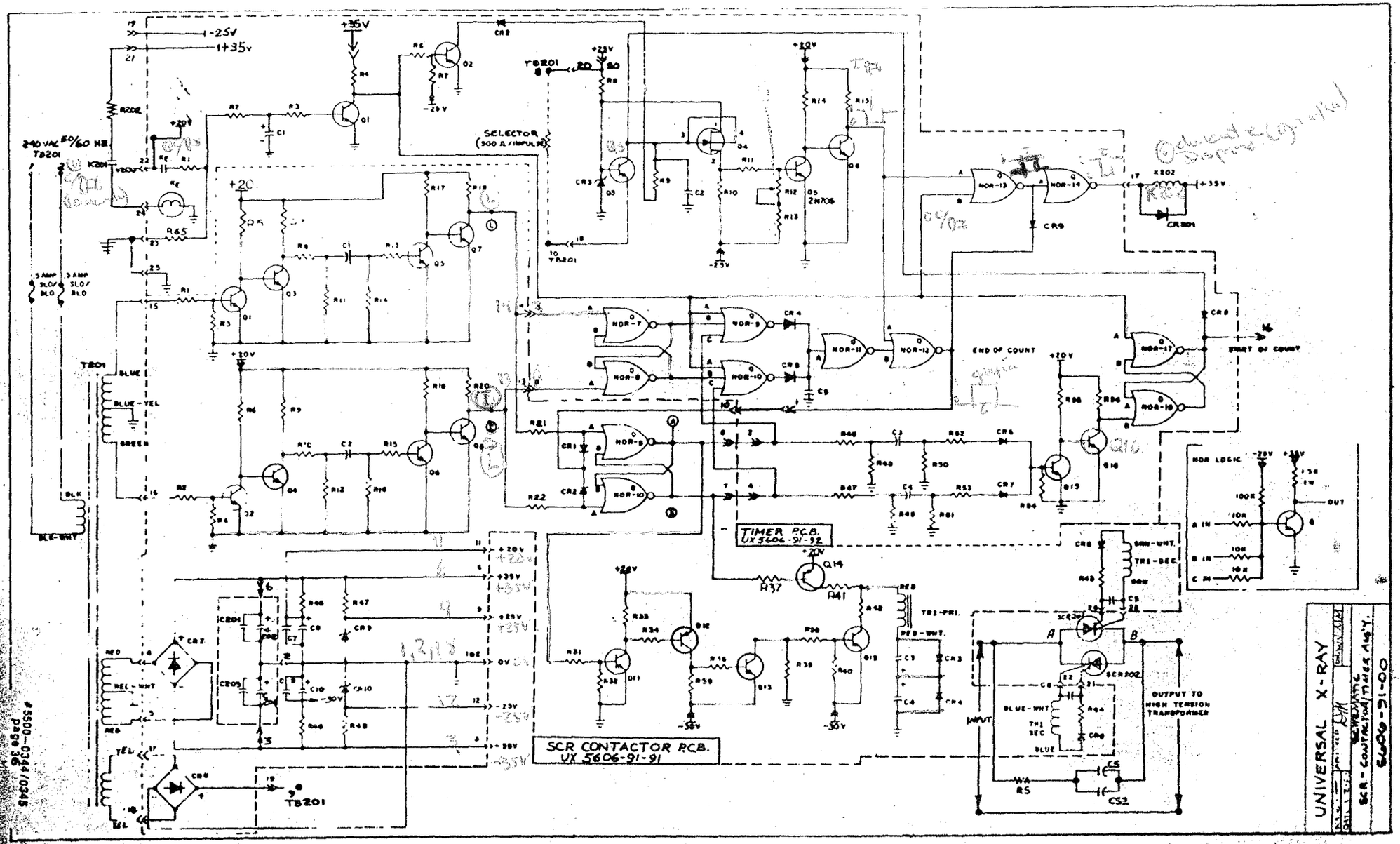
SWITCH POSITION	# OF PULSES	TIME (SEC.)	SELECTABLE RESISTOR (All 1% Resistors)
1	1	1/120	392
2	2	1/60	845
3	3	1/40	1.24K
4	4	1/30	1.87K
5	5	1/24	2.32K
6	6	1/20	2.74K
7	8	1/15	4.02K
8	10	1/12	4.99K
9	12	1/10	5.9K
10	18	3/20	9.09K
11	24	1/5	12K
12	30	1/4	15K
13	36	3/10	18K
14	48	2/5	23.7K
15	60	1/2	30.1K
16	90	3/4	45.3K
17	120	1	60.4K
18	150	1-1/4	75K
19	180	1-1/2	90.9K
20	240	2	121K
21	300	2-1/2	150K
22	360	3	178K
23	720	6	365K

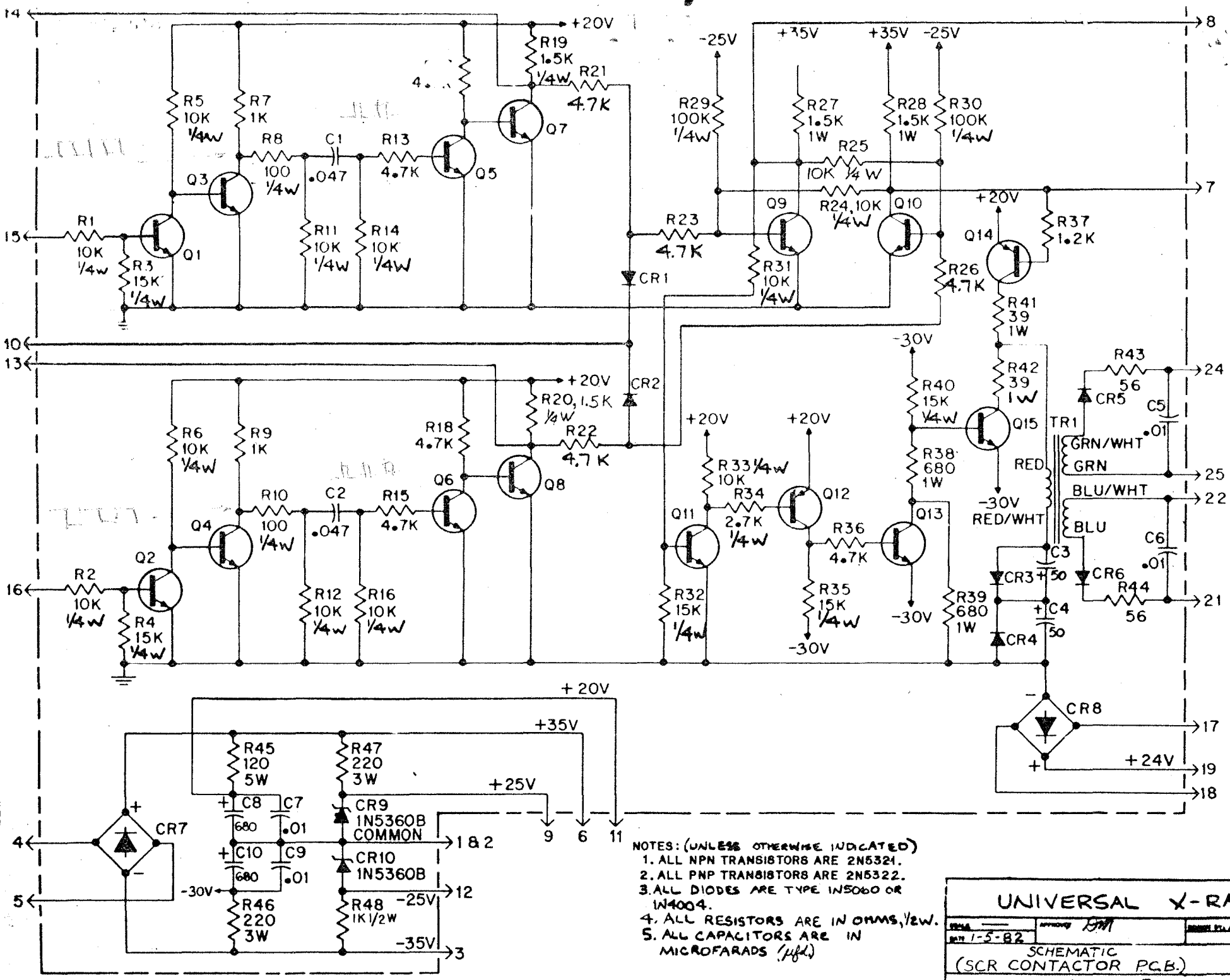


NOTES:
IF YOU ARE UNABLE TO OBTAIN AN OUT PUT. THEN REVERSE THE 246 VOLT WIRES AT TB-201 TERMINALS 1 & 2. PHASING TO LINE IS NECESSARY. AND YOU HAVE A 50/50 CHANCE OF DOING IT RIGHT RANDOMLY.

TERMINALS A AND B WIRED IN SERIES WITH PRI. SIDE OF N T TRANSFORMER

UNIVERSAL X-RAY		
SCALE: NONE DATE: 12-31-91	APPROVAL	DRN. MARK
OVERALL WIRING DIAGRAM		
		DRAWING NO. 5606-91-00


-25V
+35V
240 VAC 50/60 HZ
T8201
SELECTOR
(900 A/IMPULSE)
5 AMP SLO/BLO
3 AMP SLO/BLO
TB01
BLUE
BLUE-YEL
GREEN
BLK
BLK-WHT
RED
RED-WHT
YEL
TIMER P.C.B.
UX 5606-91-92
SCR CONTACTOR P.C.B.
UX 5606-91-91
END OF COUNT
START OF COUNT
NOR LOGIC
A IN
B IN
C IN
OUT
TR1-PRI.
TR1-SEC.
BLUE-WHT.
INPUT
OUTPUT TO HIGH TENSION TRANSFORMER
WARS
UNIVERSAL X-RAY
SCR - CONTACTOR/TIMER ASS'Y.
5606-91-00
#5500-0344/0345
page 36



NOTES: (UNLESS OTHERWISE INDICATED)
1. ALL NPN TRANSISTORS ARE 2N5321.
2. ALL PNP TRANSISTORS ARE 2N5322.
3. ALL DIODES ARE TYPE IN5060 OR IN4004.
4. ALL RESISTORS ARE IN OHMS, 1/2W.
5. ALL CAPACITORS ARE IN MICROFARADS (μfd.)

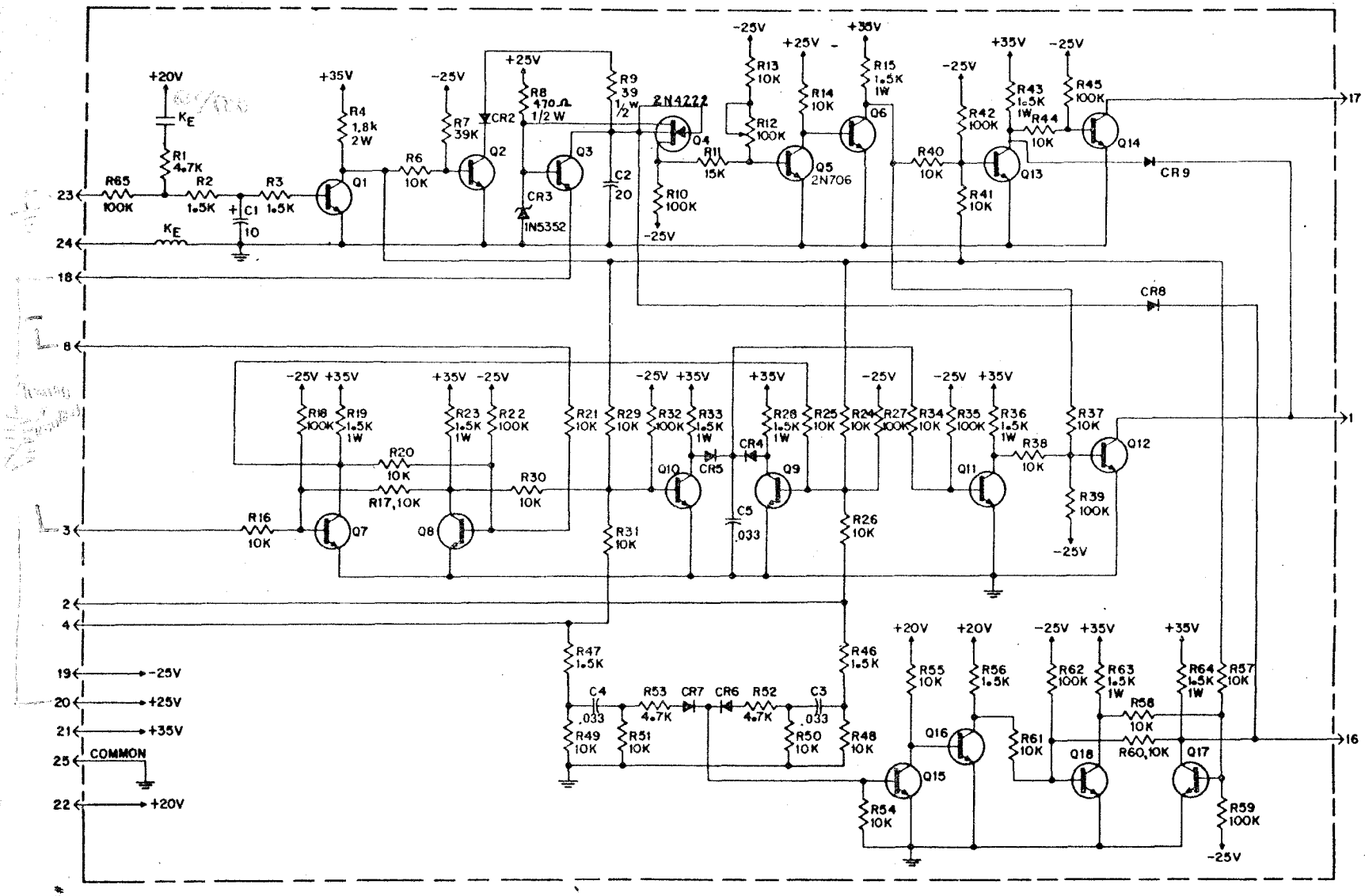
UNIVERSAL X-RAY

DATE 1-5-82

SCHEMATIC
(SCR CONTACTOR P.C.B.)

5/a0/a - 91 - 91

#5500-0344/0345
page 37



NOTE: UNLESS OTHERWISE INDICATED.

1) ALL NPN TRANSISTORS ARE TYPE 2N5321.
2) ALL PNP TRANSISTORS ARE TYPE 2N5322.
3) ALL DIODES ARE TYPE IN5060 OR IN4004.
4) ALL RESISTORS ARE IN OHMS 1/4W.
5) AL. CAPACITORS ARE IN MICROFARADS.

UNIVERSAL X-RAY		
MARK 12-31-67	APPROVED DM	SC
SCHEMATIC (TIMER P.C.B.)		
5606-91-92		

#5500-0344/0345
page 38

1 N5352 = Z. 15V 5W
se daña y no corta el disparo